ABSTRACT OF THE DISCLOSURE

Mechanisms in which a memory controller efficiently manages time-division multiple access to system memory for multiple processors and for one or more other memory consumers present in the system. At least one processor is guaranteed access to system memory during its time slot in a memory access cycle, while at least one of the other processors is only conditionally granted access to system memory during its time of the memory access cycle. In particular, these other processors are only granted access if one of more certain other memory consumers has not also requested memory access at the same time. Accordingly, urgent, time-sensitive processes may run on these guaranteed processors, while allowing less time-sensitive processes to run on the other processors. Hence, access to system memory is managed more efficiently.

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